An Analog Technique for Optimizing EPROM Programming

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MOS processes designed to accept MEMs or sensors often are not good candidates for EPROMs; nevertheless, it is desirable in this environment to have non-volatile memory capability to store circuit calibration settings. The programming speed of EPROM cells in the mentioned processes can be excessively slow, often times lasting up to tens of seconds. Since this is unacceptable for many applications, a circuit approach has been developed that compensates for the deficiency of the process by maintaining a maximum level of charge injection into the floating gate during a programming cycle. In our 2μ channel length 46.5nm gate oxide process, this method can decrease programming time by a factor of ~3.6 when compared with the conventional step voltage gate systems, and is inherently self verifying. A small 8x8 array has been realized as a drop in calibration memory, and to test the concept. Because the proposed programming method is a general optimization technique, it can be applied to a wide range of processes. It should therefore be of interest to the electron device community, since combining this circuit optimization method with advanced processing techniques can lead to even higher performance memories than would be achieved with processing alone.

By using actual gate current measurements as tabled data in combination with curve fitting techniques, an EPROM model was created, experimentally verified, and exported to the circuit simulator Hspice. The model is employed to show increase in programming speed. Fig.1 depicts the waveforms obtained during a standard programming cycle employing a step wave applied to the control gate as indicated by Vcg. ΔVt, the threshold shift, is calculated by $\Delta Vt=Vcg-(Vfg/\alpha)$, where α is the coupling coefficient and Vfg is the floating gate voltage. The gate current, which is depicted by the Ig curve below, is initially low because of a small drain E-field leading to only minimal impact ionization; but the gate field is sufficient for injection of the few available carriers into the floating gate, which in turn causes its potential Vfg to drop. When Vfg reaches the optimal voltage, the drain field supports a higher impact ionization level, yet the gate field, though reduced, is still sufficiently high so that maximum current injection occurs, a condition where Vfg nearly equals the drain voltage. If, during programming, both these voltages could be fixed at the optimal values, programming speed would be maximized. Fig.2 shows this condition. Note that Ig immediately reaches and maintains maximum injection value during programming while a step-ramp voltage waveform is formed on the control gate as charge is accumulated on the floating gate.

Fig.3 shows a conceptual diagram of the method devised to optimally set and maintain the equal floating gate and drain voltages in an EPROM cell. Since the floating gate is by necessity isolated from external circuitry, the proposed technique acts to create a phantom voltage source that fixes the potential of the floating gate without actually contacting it. A reference NMOS device shown below the EPROM cell is a replica of the floating gate transistor within the above EPROM. Note that the gate and drain are tied together at the node of a sensing resistor connected to supply Vdd. A replica sensing resistor is connected to the drain of the EPROM cell. The current set by the gate-drain connection of the reference device produces a voltage drop across the corresponding sense resistor read out as Vdref. Making Vd on the EPROM match Vdref implies both devices are carrying identical drain currents, which further implies that Vgref matches Vfg. By connecting Vd and Vdref to the depicted error amplifier, control gate Vcg will be continually adjusted as charge accumulates on the floating gate, so that Vfg remains at a fixed value, that of a phantom supply with value Vgref. Thus, Vcg forms the step-ramp that is depicted in Fig.2 to maintain a constant peak Ig. This idea has been extended to an array where all devices can be monitored with a single fully integrated feedback loop, as will be discussed in the paper. Fig.4 displays actual programming waveforms generated by the circuit controlling a typical and moderately slower device within an array. Note that the ramps both start at about the same voltage (12V). This is to be expected since there is not significantα variation among EPROM cells. The differing ramp slopes are automatically generated by the feedback action as determined by the variable maximum Ig caused by the different charge injection efficiencies. Formation of a ramp directly proves that an EPROM was programmed, since the ramp is intrinsically generated by charge injection onto the floating gate.

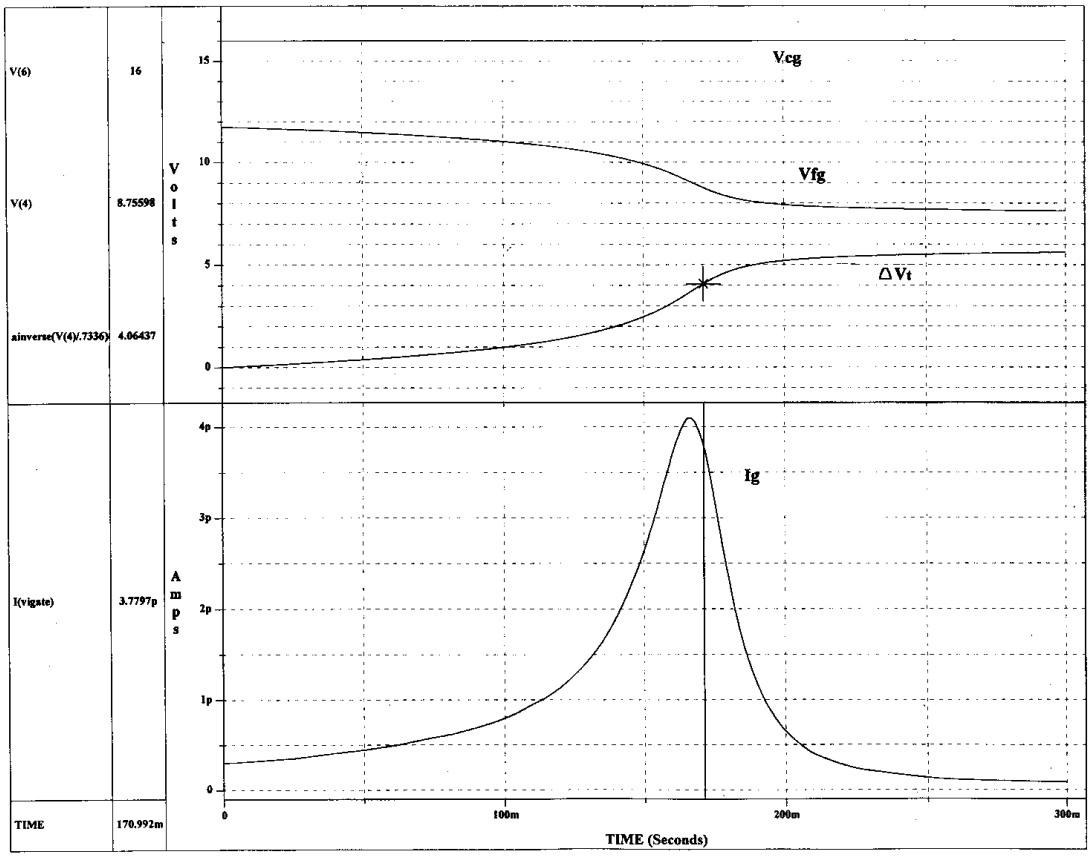


Figure 1 Standard Programming: Step Voltage Wave on Control Gate

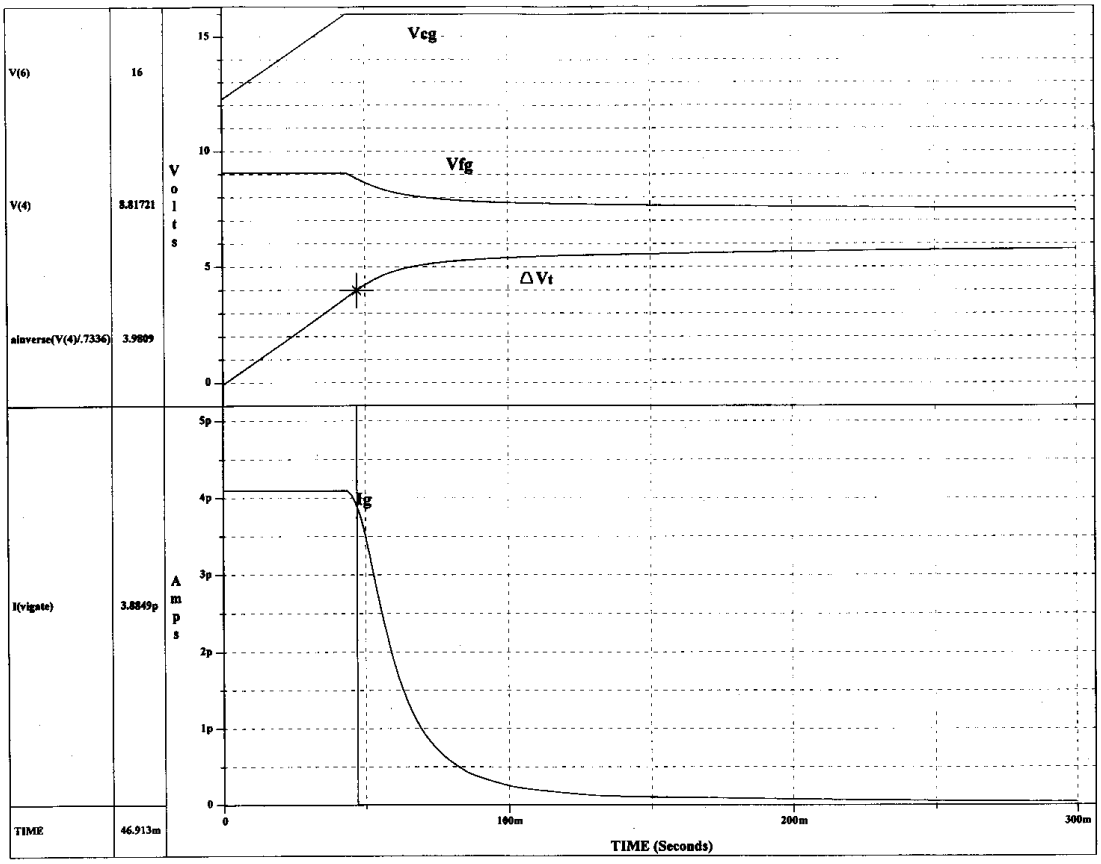


Figure 2 Programming with Maximum Charge Injection Current into Floating Gate

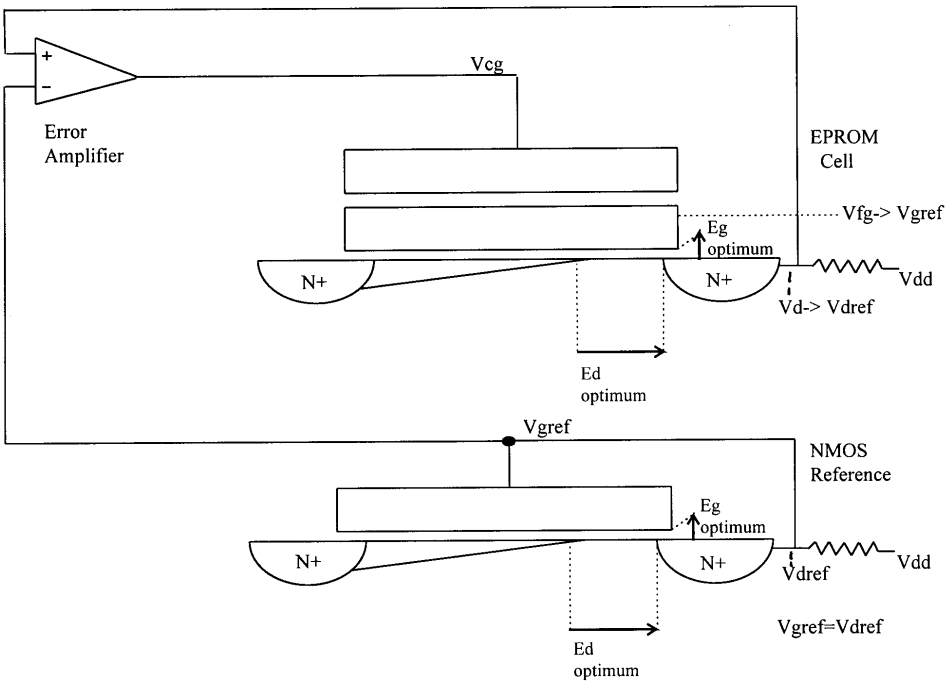
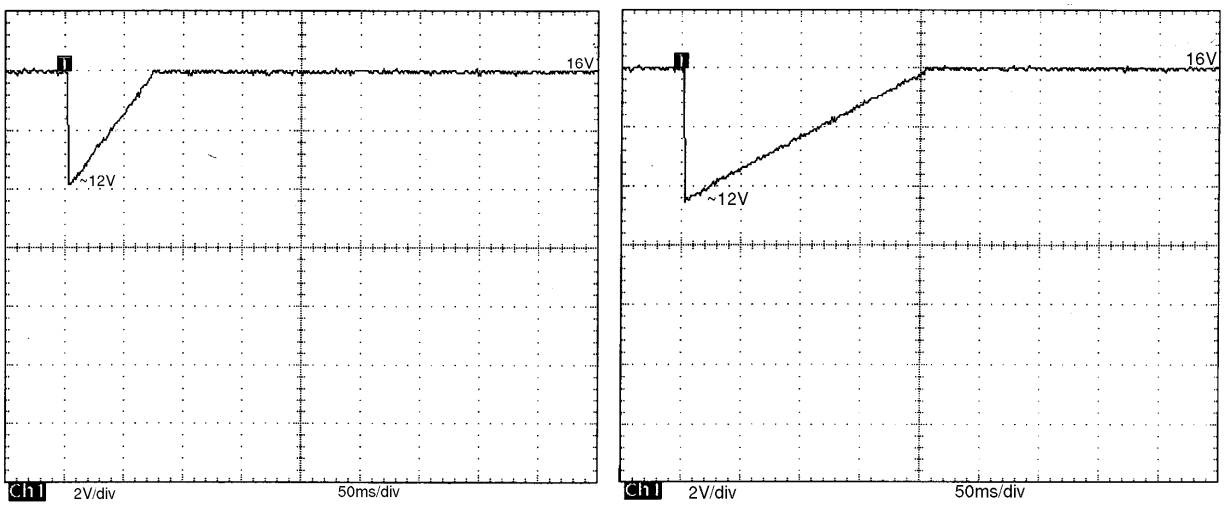


Fig. 3 Conceptual Diagram of Feedback Optimization Circuit



Typical EPROM Cell

Moderately Slow EPROM Cell

Measured Control Gate Ramp Waveforms Generated by the Integrated Feedback Loop within an Array

Figure 4