C. Andrew Lish
Aspen Scientific Design, Inc.
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Summary:

Over thirty five years of experience primarily in MOS/BiCMOS IC research and design with an emphasis in analog signal processing and MEMS. Systems experience includes R&D for adaptive filters, PLLs, and servos. Engineering/technical supervisory experience including business experience running a small consulting practice.

Experience:

4/94 – Present: Aspen Scientific Design, Inc., Nashua, NH- President. Developed navigation-sensitive MEMS magnetometer under joint DARPA/client funding which included on-chip low noise sensor detection circuit analysis/design along with the development of an original vibration modeling method for the mechanical structure. Developed microphone noise cancellation chip incorporating continuous time D/A controlled adaptive filters along with associated behavioral modeling and algorithm development. Responsible for design/system modeling of analog core of A/D converter chip. Responsible for low phase noise oscillator design, mathematical quartz crystal modeling, and frequency/temperature compensation algorithm for TCXO project. Devised proprietary control method for maximizing floating gate charge injection speed for EPROM technology development project. Devised MEMS accelerometer systems method having intrinsic stationary calibration. Designed combination chopper/CDS thermocouple amplifier for fuel cell controller. Developed mathematical definition of signal chain incorporating delta-sigma modulator for fingerprint sensor array. Developed sequence-sensitive charge injection models for MOS switch error minimization. Devised proprietary multi-phase PWM architecture for transient power management. Developed conformal mapping based sensitivity modeling for design of MEMS electrometer. Developed analytical multi-loop stability model for Li-Ion battery charger chip. Developed closed-form tensor augmented statistical modeling method for circuits/systems. Representative clients include Analog Devices, National Semiconductor/TI, IDT, Medtronic, and Fairchild Semiconductor/ON Semiconductor.

10/15 – 1/17: ASIC North, Nashua, NH (remote) – Sr. Circuit Design Engineer. Devised original 2 and 4 coil RFID backscatter reader architectures providing carrier neutralization. Derived a first principal based RFID energy harvesting optimization model using Neumann Mutual Inductance Integral for single and dual stacked on-chip antenna coils. Performed feasibility investigation for medical implant communication link which included tissue-related heating analysis.

4/91 – 4/94: Unitrode Integrated Circuits Corp., Merrimack, NH- Principal

Design Engineer. Responsible for developing major sections of servo control chip including design of proprietary floating buffer BiCMOS amplifier for inductive load. Created initial chip level architecture for DMOS disk drive actuator; designed corresponding servo amp. Responsible for dual high speed PWM switching power supply chip. Developed adaptive algorithm for NMOS impact ionization characterization project.

9/86 –12/90: Philips Laboratories, Briarcliff Manor, NY- Senior Member Research Staff. Responsible for algorithm research in Video Echo Cancellation VLSI Project. Devised general mathematical model describing tap position and value optimization in adaptive filters. Technically supervised and contributed to the design of D/A ASIC for Color TV Convergence System. Designed high frequency BiCMOS Switched Capacitor Filter to equalize HDTV signal.

10/79 – 9/86: Standard Microsystems Corp., Hauppauge, NY- Principal Engineer. Responsible for all Analog MOS at SMC: wrote initial proposal for R&D, coordinated work with processing group to modify existing digital process to accept analog circuits. Efforts resulted in creating proprietary Switched Capacitor Filter Topology with parallel structure. Developed Switched Capacitor Speech Scrambler IC. Designed data recovery circuitry for disk drives and various consumer ASICs. Technical supervisor and mentor of an engineer.

4/77 – 10/79: North Atlantic Industries, Hauppauge, NY- Asst. Development Engineer. Designed Phase Locked Loop motor servo, Back EMF velocity servos, and digital control circuitry for computer tape drives.

Patents:

8,129,964 - 2012. Interleaved/All-Phase Mode Switched PWM System. A multi-phase PWM architecture for transient power management.

5,361,041 - 1994. Improved Push-Pull Amplifier. Presents floating replica buffer technique to control NMOS source follower.

5,050,119 - 1991. Optimized Sparse Transversal Filter. Methods where tap weight position and value are both optimized.

5,043,814 1991. Adaptive Ghost Cancellation Circuit. Adaptive filter with variable weight position and value that attenuates video echo.

5,045,945 - 1991. Method of Adaptive Ghost Cancellation. Uses a threshold technique to establish tap position. (with S. Herman)

4,866,645 - 1989. Neural Network with Dynamic Refresh Capabilities. A hybrid analog-digital architecture is used.

4,697,153 - 1987. Cascode Auto-Bias Circuit. Used to automatically tune

amplifier bias for maximum output swing over MOS process spread.

4,538,113 - 1985. Switched Capacitor Filter. Linear phase type; topology developed to implement Lerner Function.

4,122,490 - 1978. Digital Chroma Key Generator. A special effects circuit that creates traveling mattes with chroma phasor of NTSC video signal.

Publications/presentations:

"A Direct Energy Balance Method for Approximating Envelope Decay of Oscillating MEMS Structures," IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, June 2004.

"A Class A/B Floating Buffer BiCMOS Power Op-Amp," IEEE Journal of Solid-State Circuits, June 1995.

"A Method of Tap Clustering in an Adaptive Filter for Video Ghost Cancellation," IEEE Intl. Symp. on Circuits and Systems Proceedings, May 1990.

"Functional-Level Simulation of Switched Capacitors with Non-ideal Switches and Operational Amplifiers," with D. Giannopoulos and S. Wong. IEEE Custom Integrated Circuits Conf. Proceedings, May 1989.

"A z Plane Lerner Switched Capacitor Filter," IEEE J. of Solid State Circuits, Dec. 1984.

"A z Plane Lerner Switched Capacitor Filter," IEEE Custom Integrated Circuits Conf. Proceedings, May 1984.

Affiliation:

Senior Member, IEEE.

Education:

1976 M. Eng. Electrical Engineering, Rensselaer Polytechnic Institute, Troy, NY
1975 B.S. Electrical Engineering, Rensselaer Polytechnic Institute, Troy, NY