FUNCTIONAL-LEVEL SIMULATION OF SWITCHED-CAPACITOR CIRCUITS WITH NON-IDEAL SWITCHES AND OPERATIONAL AMPLIFIERS

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ABSTRACT

A functional simulator has been implemented to allow switched-capacitor networks to be simulated with general analog and digital circuits. The simulator takes into account non-ideal op-amp settling behaviors, capacitive loading, switch resistances, and operate more than an order of magnitude faster than SPICE.

INTRODUCTION

To simulate analog and digital circuits involving large differences in time constants, transistor-level simulators like SPICE [1] are usually not viable due to long CPU times. Functional-level simulators with simplified circuit models are typically faster, but can be restrictive in terms of accuracy and applications. SWITCAP [2], for example, is a special purpose simulator used only for switched-capacitor (S-C) networks. Recently, a functional-level simulator has been described [3], and has been applied to simulating analog and digital circuits in power IC's with speed up to 1000X faster than SPICE. In this paper, we extended the capability of this simulator to model S-C networks, taking in account such non-ideal effects as op amp settling effects and high resistance switches. The new simulator permits circuits of the truly mixed variety (analog, digital, and S-C) to be simulated together in a reasonable time. Compared with SPICE, the new simulator requires much shorter CPU time; first, because each block is modeled at the function level rather than at the transistor level; second, because the simulator is event driven, calculations are needed only when there is a change in the waveform's slope [3]; and third, a special time-step optimizer has been incorporated into the computational algorithm.

MODEL DESCRIPTIONS

Fig.1 shows four of the basic S-C block models used by the functional simulator. Type A and B blocks represent a differential and single-ended S-C equivalent resistor elements used in many of today's circuits [4]. These blocks are described using a first order differential equation with the resistance of closed switches modeled by a real resistor. If R_1 and R_2 are the on resistances of the switches on either side of the capacitor in a type A block, for example, during the clock cycle ϕ_1 or ϕ_2, this circuit can be modeled by the equation

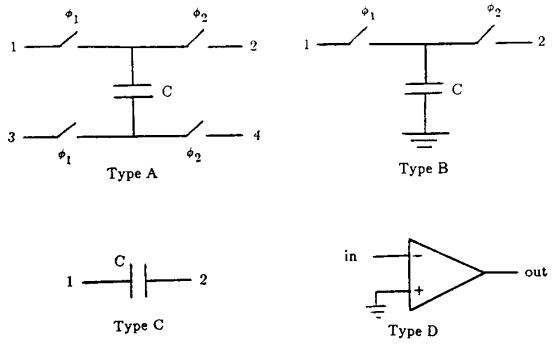

Fig. 1: Building blocks of switched-capacitor circuits.

$$v_1(t)-v_2(t)=(R_1+R_2)\frac{dq_C(t)}{dt}+\frac{q_C(t)}{C} \quad (1)$$

where $v_1(t)$ and $v_2(t)$ are the instantaneous voltages at the external nodes of the closed switches, and q_C is the instantaneous charge stored on the capacitor. During the short instances when all four switches are open, q_C is assumed constant. The equivalent model for type B blocks can be obtained from equation (1) by setting $R2$ and $v_2(t)$ to zero. For type C blocks, which model linear capacitors, the characteristic equation is given by

$$v_1(t)-v_2(t)=\frac{q_C(t)}{C} \quad (2)$$

Type D blocks are the op amp models, each combines a small signal two-pole model with a large signal slew model, and is capable of taking into account the changing loading effects by switches and capacitors during the switching cycles.

In the small signal regime, the op amp parameters are linearized so that a simple two-pole (and one zero) model can be used. This is sufficient to capture the worst-case op amp's settling behavior which can result either from large switch on-resistance or poor phase margin. The transfer function of the model is described by

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$$\frac{out(s)}{in(s)} = -\frac{k(sz+1)}{(sp_1+1)(sp_2+1)} \tag{3}$$

where k is the open-loop DC gain, $1/z$ is the zero frequency, and $1/p_1$ and $1/p_2$ are the dominant and secondary pole frequencies of the operational amplifier. To evaluate the solution in the time domain, equation (3) can be rewritten in the form

$$p_1 p_2 \frac{d^2 out(t)}{dt^2} + (p_1 + p_2)\frac{dout(t)}{dt} + out(t) = -kz\ \frac{din(t)}{dt} - k\ in(t) \tag{4}$$

In a 2-stage operational amplifier, where capacitor C_C is used as the compensation capacitor, the location of the dominant and secondary poles can be approximated by

$$p_1 = -\ g_{m2} R_o R_1 C_C \tag{5}$$

$$p_2 = -\left(\frac{C_L}{g_{m2}} + \sum_{i=1}^{n} R_{on,i} C_i\right) \tag{6}$$

$$z = C_C\left(\frac{1}{g_{m2}} - R_C\right) \tag{7}$$

where R_1 and R_o are the output resistance of the first and second stage respectively and g_{m2} is the second stage's transconductance. C_i, $R_{on,i}$, i=1,2,...n are the capacitances and the switch on-resistances of the type A and B type blocks that are connected to the output node of the operational amplifier. This is shown schematically in Fig. 2. C_L consists of the sum of all linear capacitors (block C) tied directly to the output node of the operational amplifier. As a worst-case approximation, this would include all capacitors tied directly to both real ground and to virtual grounds, and would include such loads as the feedback capacitors. On the other hand, any capacitors tied indirectly via switches (blocks A and B) are not considered as C_L but are accounted for by the term $\sum_{i=1}^{n} R_{on,i} C_i$ in equation (6), which models the effect of loading by S-C equivalent resistors on the secondary pole $1/p_2$.

The two-pole model automatically converts to a large signal slewing model when the op amp's input signal exceeds the value of I_{bias}/gm. In the large signal regime, the op amp's output characteristic is described by its rise and fall slew rates, that is,

$$\frac{dout(t)}{dt} = rslew\ or\ -fslew \tag{8}$$

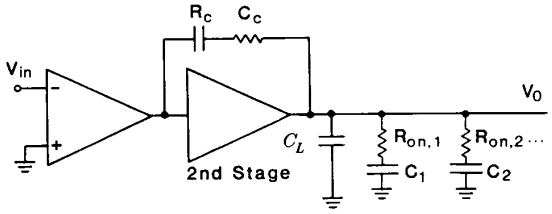

Fig. 2: Equivalent small signal model of a 2-stage op amp with loading.

The concept of virtual ground can no longer be assumed because feedback is generally not present to keep the voltages across the op-amp input terminals the same. In such cases the load contribution of the feedback capacitor is decreased by the serial connection of any capacitors which may be tied to it. This normally includes capacitors that are connected to the input of the operational amplifier either directly or through switches. All capacitors, including those tied via switches to the output node of the operational amplifier, are treated as valid load capacitances.

CIRCUIT FORMULATION

By using the four S-C blocks considered and a systematic approach to formulation, we can ensure of a necessary number of differential equations to adequately solve the system unknowns. Let n_v be the number of terminal nodes of the S-C building blocks, and n_q be the number of S-C equivalent resistors, by defining the unknown variables as the voltage at each of these nodes and the charge across each of these S-C equivalent resistors, a total of n_v+n_q unknowns are generated.

At each of the n_v terminal nodes, except where it is the output node of an operational amplifier, one can write the charge conservation equation

$$\Sigma_i q_{C_i} + \Sigma_j q_{C_j}(t) = constant \tag{9}$$

The first sum of the equation includes the fixed capacitor charges stored from the previous clock cycle of all type A and type B blocks that are tied to that node. The second sum of the equation includes the dynamic charges of all linear capacitors. Substituting in equation (2) for each of the linear capacitors yields

$$\Sigma_i q_{C_i} + (v_j(t) - v_{node}(t))C_j = constant \tag{10}$$

where v_{node} is the voltage of the node under consideration, and v_j is the voltage of the other node of the linear capacitance C_j. Using the remaining op amp output nodes, additional equations can be determined from either equation (4) or equation (8), depending on whether the input signal is smaller or greater than I_{bias}/gm. Together, they form a system of n_v equations in n_v+n_q unknowns.

From the n_q S-C equivalent resistors of the network, an additional n_q equations can be generated using equation (1). This results in a combined total of n_v+n_q system equations in n_v+n_q unknowns, to be solved for every clock phase of the S-C switching cycle.

SIMULATION EXAMPLES

Several simulation examples involving non-ideal modeling conditions are presented. In Fig. 3, a simple S-C integrator is described using the functional models. Table 1 lists the relevant block parameters where parameters rslew, fslew, k, 1/p1, 1/p2 and 1/z denote respectively the rise and fall slew rates, the dc gain, and the associated poles and zero the op amp. Fig. 4 shows the output step response provided by the functional simulator (a), comparing it with that of SPICE (b), and SWITCAP (c). Note that only in curves (a) and (b) have the overshoot behavior of the waveform been adequately captured. In general, the degree of matching will depend on the accuracy of the block parameters. In this example, SPICE took 50s in CPU time while the functional simulator took only 3.4s on a VAX-8600 computer, about a 15X improvement. In examples where the occurrence of instantaneous feedbacks is less, where simultaneous equations are needed to describe only part of a circuit, much greater speed advantage is possible. In Fig. 5, the effect of large switch resistance on S-C behavior is demonstrated. As the resistances are increased 10 fold, the incomplete transfer of charges resulted in an accumulated error of about 10%. In Fig. 6, a third simulation example is described where a second-order S-C filter is combined with a purely analog antialiasing front-end. The effect of inadequate op amp settling on the output responses is shown in Fig. 7. With a clock to signal frequency ratio kept at 100:1, case (c) demonstrated a large phase and gain deterioration when f_{clk} exceeded the op amp's gain-bandwidth frequency.

Block	Parameters	Values
A_1	R_{on}	7kΩ
	C	2pF
C_{11}	C	6pF
C_{12}	C	10pF
D_1	rslew	6V/μs
	fslew	6V/μs
	I_{bias}/gm	0.3V
	k	70dB
	1/p1	2.4KHz
	1/p2	2.4MHz
	1/z	>10MHz

TABLE I: Block Parameters

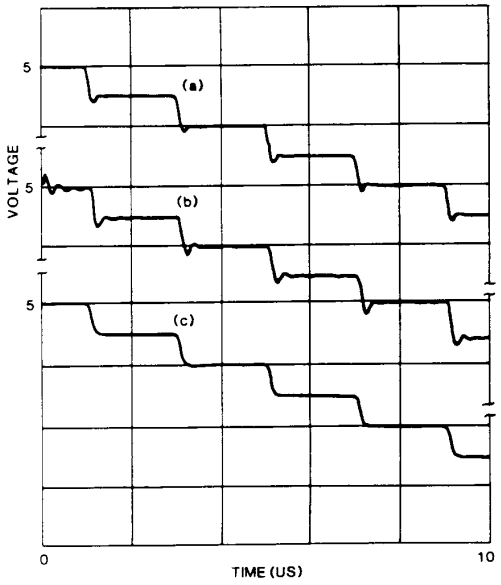

Fig. 4: Simulated integrator's waveforms using (a) functional simulator, (b) SPICE and (c) SWITCAP.

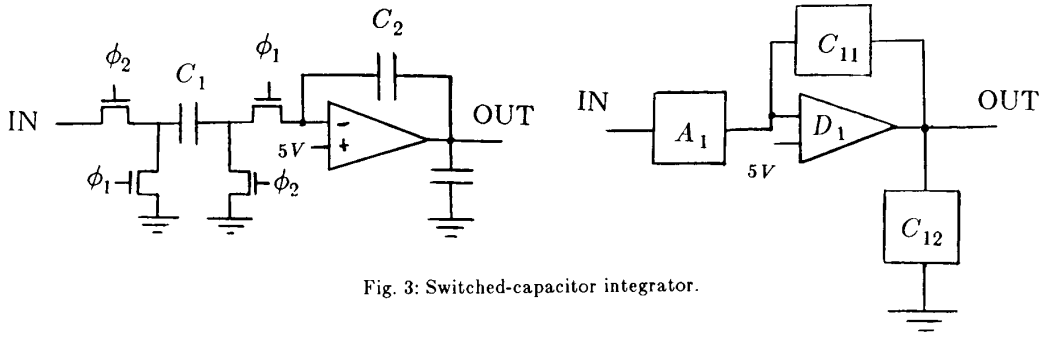

Fig. 3: Switched-capacitor integrator.

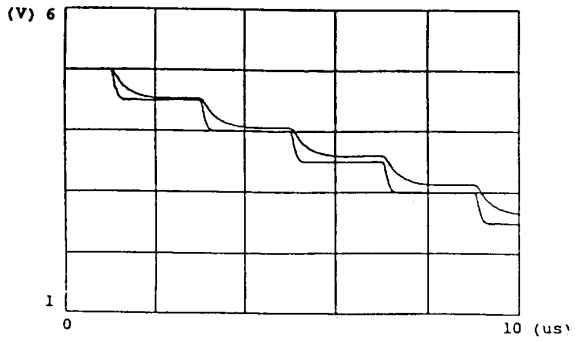

Fig. 5: Output waveforms simulated with different switch resistances.

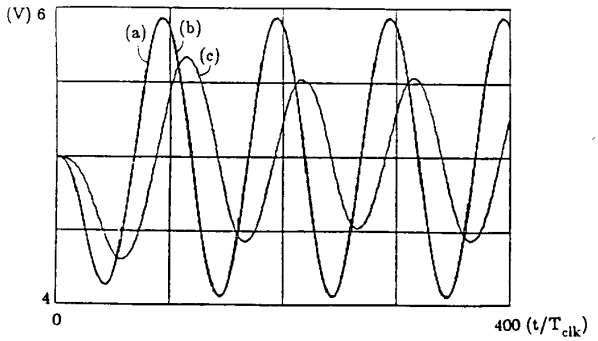

Fig. 7: Simulated output waveforms of filter with f_{clk} equals (a) 100 KHz, (b) 1 MHz, and (c) 5 MHz.

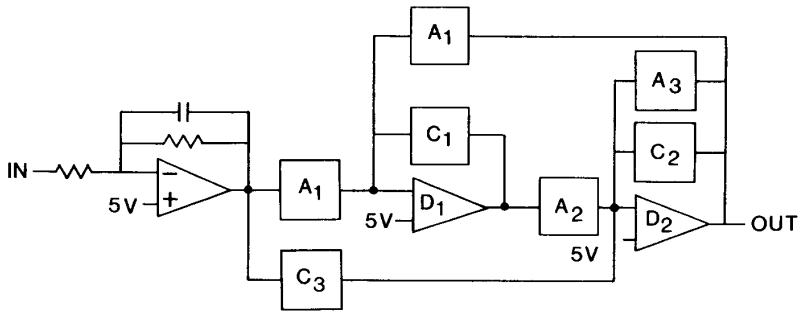

Fig. 6: Second order S-C filter with antialiasing front end.

CONCLUSION

We have presented a new functional-level simulator primarily aimed at solving switched capacitor networks. The simulator takes into consideration the on resistance of the switches as well as the op-amp settling behavior as affected by different loading conditions at both the small signal and large signal domains. Typical simulation examples of S-C circuits have yielded results compatible with those of SPICE but are obtained at a speed more than one order of magnitude faster than SPICE. In applications where the majority of the circuitry contains little or no instantaneous feedback loops, up to 1000X speed improvement over SPICE is achievable as reported in [3].

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