

A Class A/B Floating Buffer BiCMOS Power Op-Amp

C. Andrew Lish, *Member, IEEE*

Abstract—A class A/B BiCMOS power op-amp designed to drive the L/R load of a disk drive head actuator is presented. The amplifier uses totem pole NMOS outputs instead of bipolar devices to avoid the high collector resistance in the simplified process used. A unique floating buffer technique regulates the quiescent totem pole current of the output devices and provides control for deep triode NMOS operation. The amplifier is capable of driving a load in all four V - I quadrants without a deadband during transition, and achieves a 0.25 A drive capacity into a $7.5\text{-}\Omega$ load using a 5-V supply.

I. INTRODUCTION

IN THIS PAPER we present a class A/B power op-amp that is capable of driving the inductive load of a disk drive head actuator motor. Because disk drives are essentially becoming a commodity in the personal computer market, it is desirable to use an inexpensive process with a high level of integration. Thus, the BiCMOS process used for the amplifier does not have a buried layer or sinker structure for the NPN transistors; this results in excessively high collector resistance. Therefore, instead of using bipolar devices, the power output structure is an NMOS totem pole. The circuitry that drives the NMOS devices must be able to provide the four quadrant V - I control needed for an inductive load while simultaneously regulating the quiescent current so that there are no deadbands during quadrant transitions. A previous driver method [1] uses source monitored sensfets to sense and control the power NMOS currents. Because a voltage is dropped across the source monitoring resistor, an error in current sense value results (since the NMOS output and sensfet are no longer acting strictly ratiometrically). Instead of using a source monitored sensfet, our topology provides NMOS control by using a replica bias scheme incorporated into a floating buffer circuit. The device serving as the replica has its gate and source voltage matched to that of the corresponding power output device during quiescent operation; thus source voltage error is avoided. Note that current monitoring within the op-amp is used for quiescent control and not to sense load current. The modular design approach of the chip that our op-amp is part of calls for a separate instrumentation amplifier block with its input coming from a small sense resistor in series with the load.

The paper is organized as follows. First, we derive the floating buffer circuit from the classical emitter follower. We then expand this concept and explain the amplifier system.

An additional circuit is described that fine tunes the quiescent current variations in the NMOS totem pole caused by component random offsets. Results are presented showing a class A/B amplifier capable of providing 0.25 A drive capacity and 3.8 V swing into an inductive load, from a 5-V supply. The amplifier may be integrated with a twin to form a balanced H bridge topology, thus doubling the voltage swing across the load.

II. DESIGN

The NPN emitter follower ($I1$, $D1$, and $Q1$) in Fig. 1(a) has the following equation:

$$I2 = nI1 \exp\left(\frac{V'_0 - V_0}{V_T}\right). \quad (1)$$

This circuit effectively has two inputs, $I1$ and $V' - V_0$. The first sets the emitter quiescent current $nI1$, which is taken up by the PNP circuitry below when the output of the follower combination is neither sourcing nor sinking. The second input exponentially multiplies the quiescent current in response to a voltage difference when the follower is called upon to source current. Thus, the follower can be considered a local current servo that simultaneously sets a quiescent current for class A/B operation. The NMOS follower of Fig. 1(b) is similar to the NPN circuit discussed above, but has an additional region of operation that needs to be addressed (i.e., the triode mode). First, we look at the follower in saturation.

$$I_{d4} = nI1 \left[\frac{(V'_0 - V_0) + V_E}{V_{DSAT8A}} + 1 \right]^2. \quad (2)$$

In (2) consider that $V_E = 0$ initially and that there is a bottom half circuit in Fig. 1(b) that acts similarly to the top half. Note that when the circuit is in quiescent state, current $nI1$ is absorbed by the bottom half circuit. During current sourcing, the current multiplication caused by the increase of $V'_0 - V_0$ is not as dramatic as the exponential function in (1). If $V'_0 - V_0$ is augmented by controlled voltage source V_E such that $V_E = A_V(V'_0 - V_0)$, the weakness of (2) can be compensated for. In addition, this augmentation provides a means for the gate voltage to be raised above the drain supply (by $V_g \gg V_{DD} + V_T$) so that the follower may be operated in the deep triode region, a mode where high sourcing currents may be obtained with a small V_{DS} drop and the NMOS device size can be minimized. Fig. 1(c) shows the floating buffer scheme used to provide augmentation voltage V_E . Note that an on chip boost regulator will supply 15 V to the buffer so

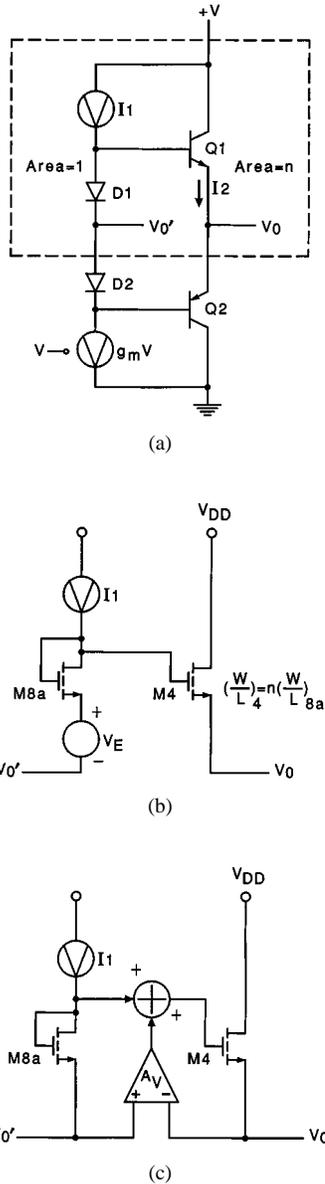


Fig. 1. Floating buffer derivation.

that the NMOS gate can be raised above $V_{DD} = 5$ V. The buffer gain is A_V and $M8a$ is a scaled down floating replica of $M4$. The transistor in triode mode can be modeled as a resistor of value

$$R \approx \frac{L_4}{2K'W_4(1 + A_V)(V_0' - V_0)}. \quad (3)$$

The V_{DSAT} of the floating replica does not appear in (3) since it is a small component of the gate drive. Also, (3) becomes more accurate when V_0 is at maximum source voltage. In fact when $V_0' = V_{DD} = 5$ V, the maximum source voltage, $V_0 = V_{0MAX}$, relates the maximum gate drive voltage V_{GMAX} to A_V .

$$A_V = \frac{V_{GMAX} - V_0' - V_{GS8a}}{V_0' - V_0}. \quad (4)$$

The buffer gain is sized to provide slightly more than the maximum gate drive needed by inflating A_V to account for process and temperature spread (i.e., put $A_V =$

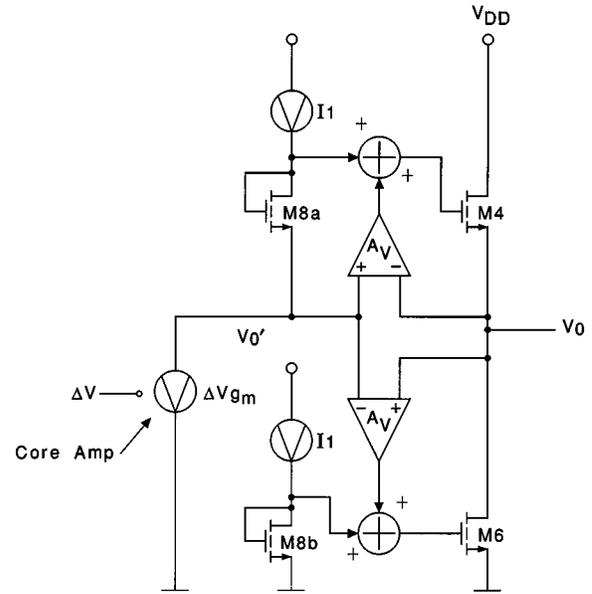


Fig. 2. Simplified amplifier.

g_m (minimum) $\times r_o$ (minimum) so that nominal g_m and r_o yield a somewhat larger gain than required). Excessive gain will increase error voltage on the gate of the NMOS output created by random offsets in the buffer circuit. We will deal with this more later. The maximum source current is used to calculate the minimum R during V_{0MAX} and W_4/L_4 is calculated without difficulty using (3).

Referring to Fig. 2, the floating replica source follower can be seen embedded in a simplified diagram of the complete op-amp. Re-arranging the components of the floating replica system creates the common source output sink using $M6$. The quiescent current in $M6$ matches that of $M4$. Since the common source circuit is similar to that in the literature, [2] we limit the discussion. The core amp transconductor equivalent shown in Fig. 2 gives the circuit its op-amp characteristics; more detail will be given later. Fig. 3 is the detailed system level diagram of the amplifier that contains the buffer and core cells with other related circuitry that will be discussed.

The detailed buffer cell (or circuit) of Fig. 4 contains the following elements depicted in Fig. 2: A buffer amplifier (A_V), a replica device ($M8$), a current source to bias the replica device ($I1$) and a voltage summer. As in Fig. 2, the two inputs to the summer are always the output of the buffer amp and the gate/drain of the replica device; thus this functionality is fixed in the detailed buffer circuit of Fig. 4. The inputs to the buffer amp are V_{IN+} and V_{IN-} . The connection of the source of the replica is node R . When the buffer circuit is floating so as to drive the NMOS source follower, R is connected to the output of the core amp. For the second buffer circuit used to control the bottom NMOS common source output, R is connected to ground. The output voltage at the emitter of $Q22$ matches the voltage at the drain of the replica device $M8$ when the positive and negative inputs of the buffer are equal. This is because there is no voltage drop across the loop consisting of $Q80$, $R1$, $Q82$, $Q84$, $R2$, and $Q22$. A base current compensation circuit, in Fig. 4, having an output at

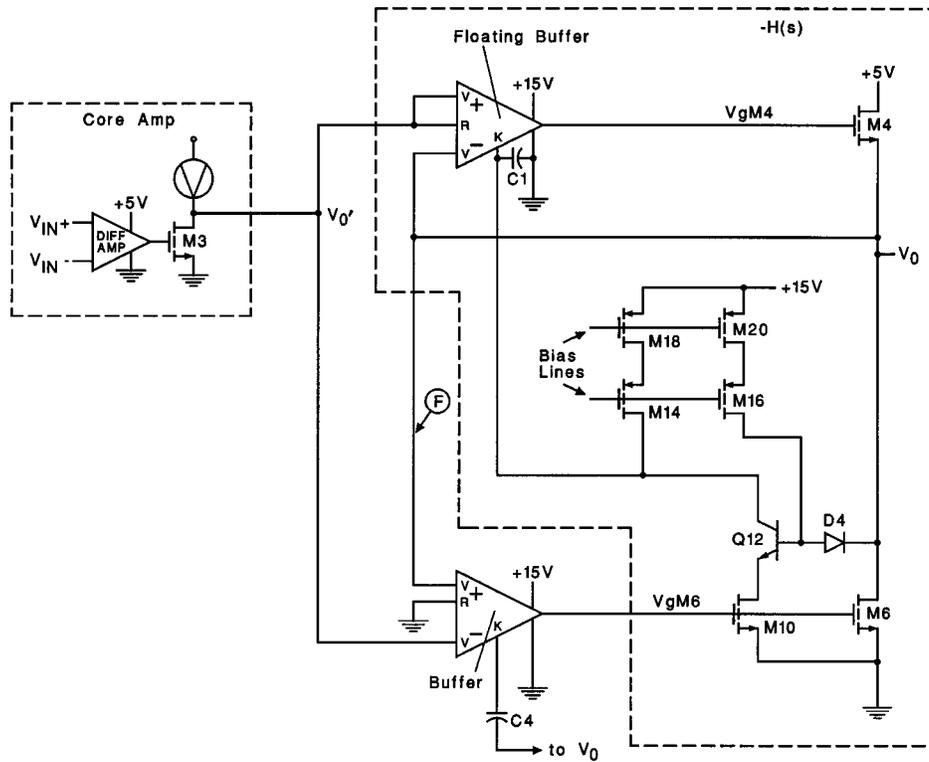


Fig. 3. Detailed amplifier system.

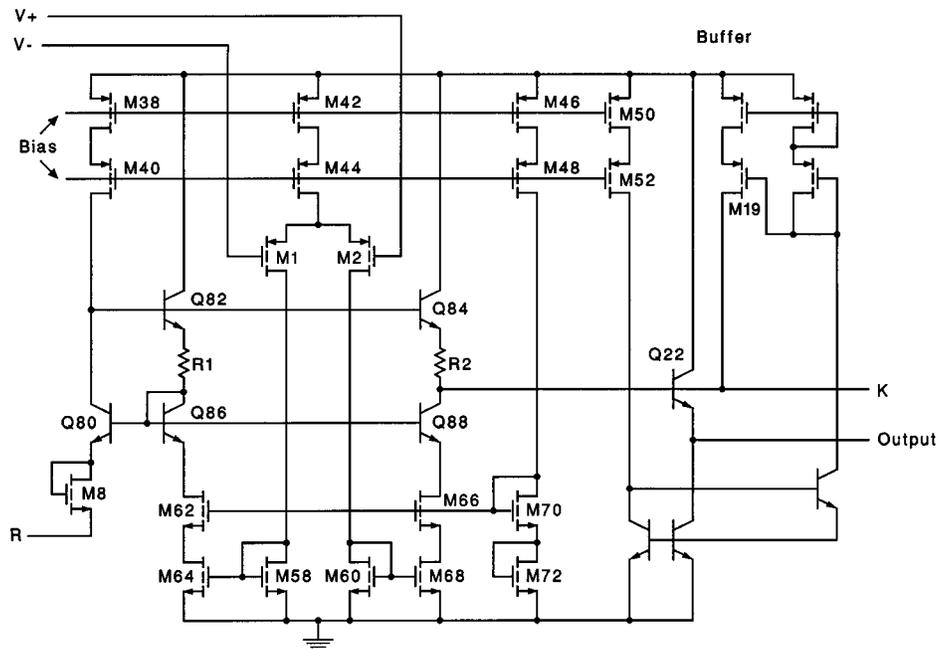


Fig. 4. Buffer.

the drain of $M19$ equalizes the base load of $Q22$ to $Q80$. The amplifier within the detailed buffer circuit has a gain of $g_{m1}R1$, assuming $M1$ matches $M2$ and $R1$ matches $R2$. Note that the summation of the replica voltage with the amplifier takes place because of superposition. The full ac voltage gain is realized at high impedance node K . Compensation of the upper buffer is accomplished by $C1$ tied to ground and K . For the lower buffer, $C4$ is tied between K and the drain of the

lower power NMOS device. This is done because the g_m of that device varies with the current it is sinking through the load inductor and pole splitting compensation maintains a constant $GBP = 10$ MHz (the top buffer also has $GBP \approx 10$ MHz). In order for the power output to slew at 1 V/ μ s, as determined by the core amp, both upper and lower buffers need to slew the power gates at ≈ 20 V/ μ s when in deep triode operation. If the core were able to call for a greater slew rate, cross conduction

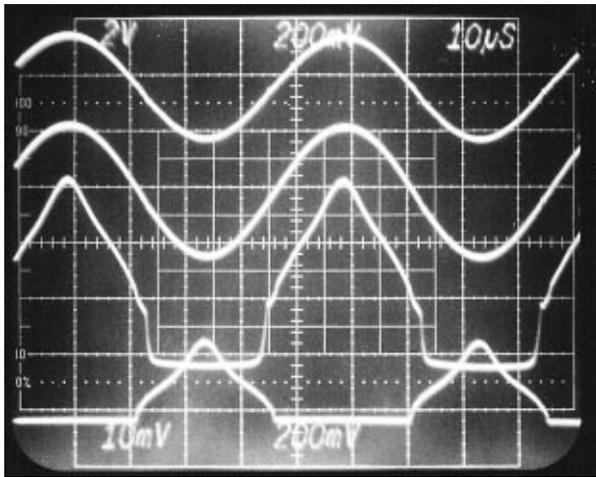


Fig. 6. Resistor load traces.

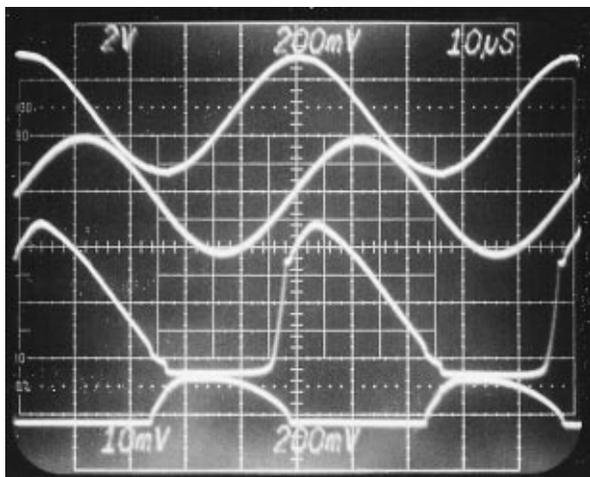


Fig. 7. Inductor load traces.

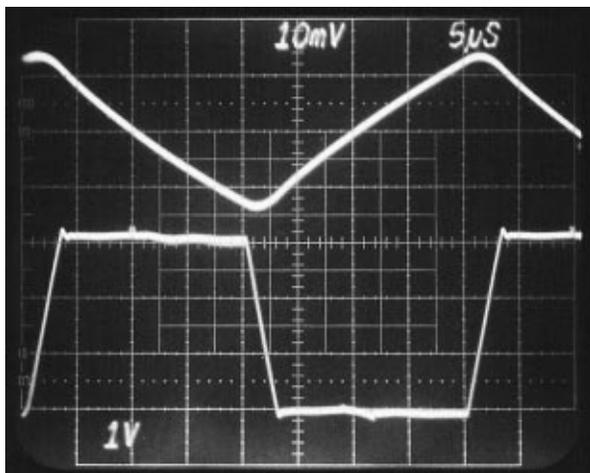


Fig. 8. High frequency square wave response with inductor.

rails. Table I gives some measured parameters of the power op-amp. When a second identical on chip op-amp is used in a balanced H bridge configuration, the voltage swing across the load is doubled. A power of 0.5 W_{rms} can be supplied to the load in this fashion. Fig. 9 is a die photo of a single power op-amp.

TABLE I
CIRCUIT PARAMETERS

Item	Value	Comments
Process		3 μ BiCMOS
Size	1850 mil ²	
V_{DD}	5 V	Note: Calculated Core Amp IDD = 165 μ A
V_{BOOST}	15 V @ 1.45 mA (calculated)	Buffer Supply
$V_{DD} - V_{0MAX}$	540 mV	Source 250 mA
V_{0MIN}	632 mV	Sink 250 mA
Slew Rate	1 V per μ s	
GBP	3.3 MHz*	
THD	0.5%*	3.4 V p - p into 7.5 Ω
$I_{TOTEM POLE}$	\approx 1 mA	

*Extrapolated from preliminary measurements

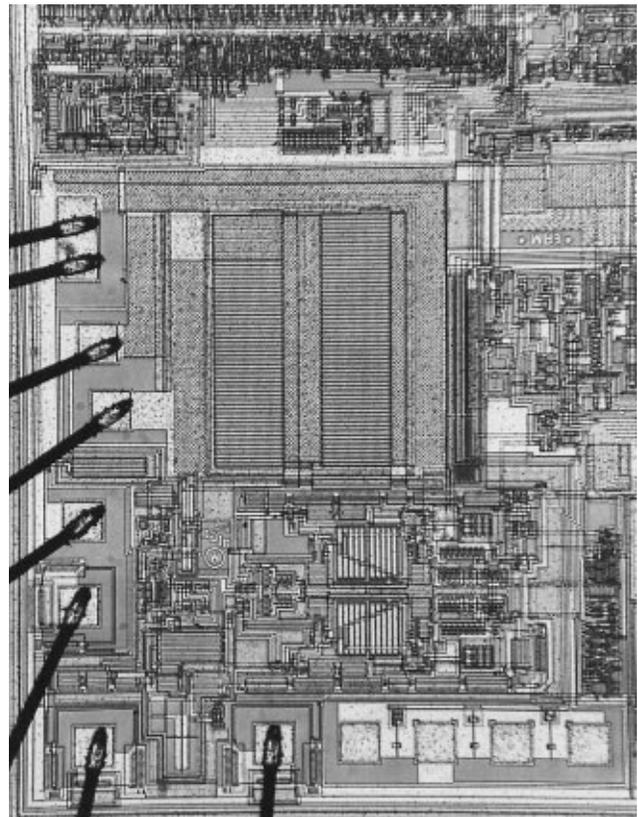


Fig. 9. Die photo.

IV. CONCLUSION

In this paper we have presented a power op-amp designed to drive the $L-R$ load of a disk drive head actuator. Because the NPN devices in the simplified BiCMOS process have high collector resistance, the amplifier's power output structure is an NMOS totem pole. A unique floating buffer circuit controls the totem pole's quiescent current while simultaneously providing gate drive necessary for deep triode operation. Thus, the four $V-I$ quadrants encountered when powering an inductive load are transitioned without a deadband. While the systematic quiescent current is set by replica scaled down power devices embedded within the floating buffer (and fixed bottom buffer), variation in quiescent current caused by random component mismatch is fine tuned by a cross current feedback circuit.

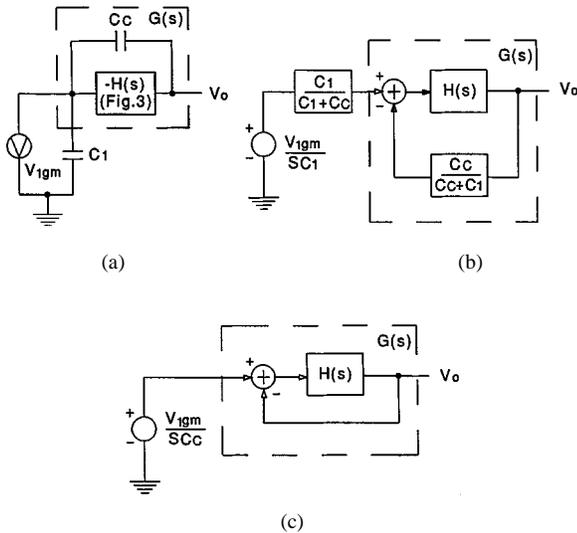


Fig. 10. Pole split derivation.

The results presented show that a high performance power op-amp is practical in a simplified BiCMOS process.

APPENDIX

As mentioned in the main text, the cross current loop is embedded within the pole split loop of the lower buffer circuit. This can be analyzed as an arbitrary transfer function within a pole split loop by creating a very simple intuitive model. Fig. 10(a) shows a pole split loop formed around function $-H(s)$ by compensation capacitor C_C . We assume that the resistive impedance of the first stage is infinitely high and the output of the second stage is zero impedance. By using simple Thevenin equivalent modeling, Fig. 10(a) may be mapped into Fig. 10(b). Thus, the pole split circuit is viewed as a classical feedback system. When $C_C \gg C_1, C_C/(C_C + C_1) = 1$. This allows Fig. 10(b) to be further reduced to Fig. 10(c). Note that all the assumptions mentioned are applicable to the cross current circuit; some accuracy is sacrificed to gain insight.

The circuitry enclosed by the dashed outer polygon labeled $-H(s)$ in Fig. 3 corresponds to the $H(s)$ of Fig. 10(c). The dominant pole and zero of $H(s)$ is shown in Fig. 11(a) along with their related expressions. gm is the transconductance of M_4 and M_6 , gm_1 is the transconductance of each of the buffer input transistors, C is the value of the compensation capacitors for both buffers, R_2 is the buffer load resistor (see Fig. 4), and variable K is the ratio of M_{10} to M_6 (see Fig. 3). Closing the loop around $H(s)$ yields $G(s)$ as shown in Fig. 10(c). This, of course, moves the pole of $H(s)$ towards the zero. Fig. 11(b) depicts this along with the integrator pole added by the controlled voltage source of Fig. 10(c). The Bode plot of Fig. 11(c) contains the poles and zero of Fig. 11(b). To complete the cross current loop analysis, V_1 is made equal to V_0 of Fig. 10(c) by the connection of branch F as shown in Fig. 3. Thus, $G(s)$ is nested within a larger loop that is easily analyzed with the Bode plot. The cross current feedback coefficient corresponding to Fig. 11(c) is 1.66 and is proportional to the variable K . Clearly, this loop is stable.

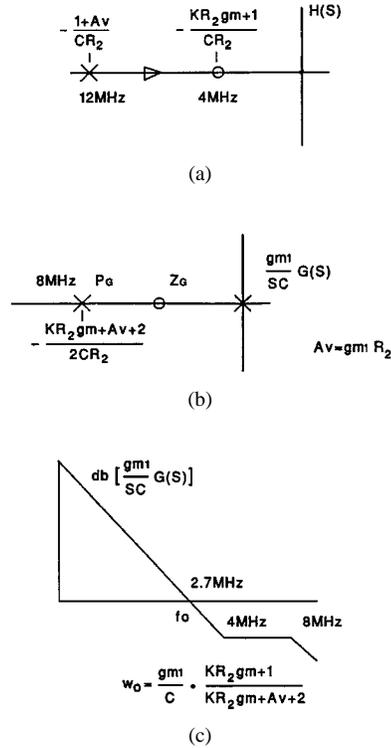


Fig. 11. Current analysis.

To understand the effect of increasing the cross current feedback coefficient, we refer again to Fig. 11. At $K = 0.0017, |Zg| < |Pg|$; this is where our circuit is set. As K is increased, the $|Zg|$ will pass $|Pg|$ in frequency. The Bode plot would then have a -40 db/decade section in it occurring beyond $|Pg|$. But since $|Pg| > \omega_o$ when the zero passing occurs, the -40 db section is below the 0 db line and stability is assured. Interestingly, with the parameters $R_2, gm,$ and gm_1 used in the circuit, $|Pg|$ will always exceed ω_o for K being arbitrarily large, and ω_o will not exceed the GBP of the buffers. There are other effects not covered in this simplified explanation (i.e., nonlinearities, loading, etc.) but simulations have worked with K being 10 times the value used in our circuit. This corresponds to K being 2.5 times where the zero passes the pole.

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C. Andrew Lish (M'80) was born in New York in 1953. He received the B.S.E.E and M.Eng.E.E. degrees from Rensselaer Polytechnic Institute, Troy, NY, in 1975 and 1976, respectively.

He is currently President of Aspen Scientific Design Inc., Nashua, NH, acting as a Private Consultant with primary practice in analog signal processing integrated circuits. From 1991–1994, he was a Principal Engineer at Unitrode Integrated Circuits, Merrimack, NH, responsible for developing disc drive circuitry. From 1986–1990, he was a Senior

Member Research Staff for Philips Laboratories, Briarcliff Manor, NY where he developed algorithm mathematics for adaptive cancellation of video ghosts. Before Philips he was a Principal Engineer with Standard Microsystems, Hauppauge, NY where he initiated and performed research, development and design of analog MOS signal processing IC's.

Mr. Lish holds eight patents and has published several IEEE papers.